**CA Lab class – Class on Verilog 2/11/16**

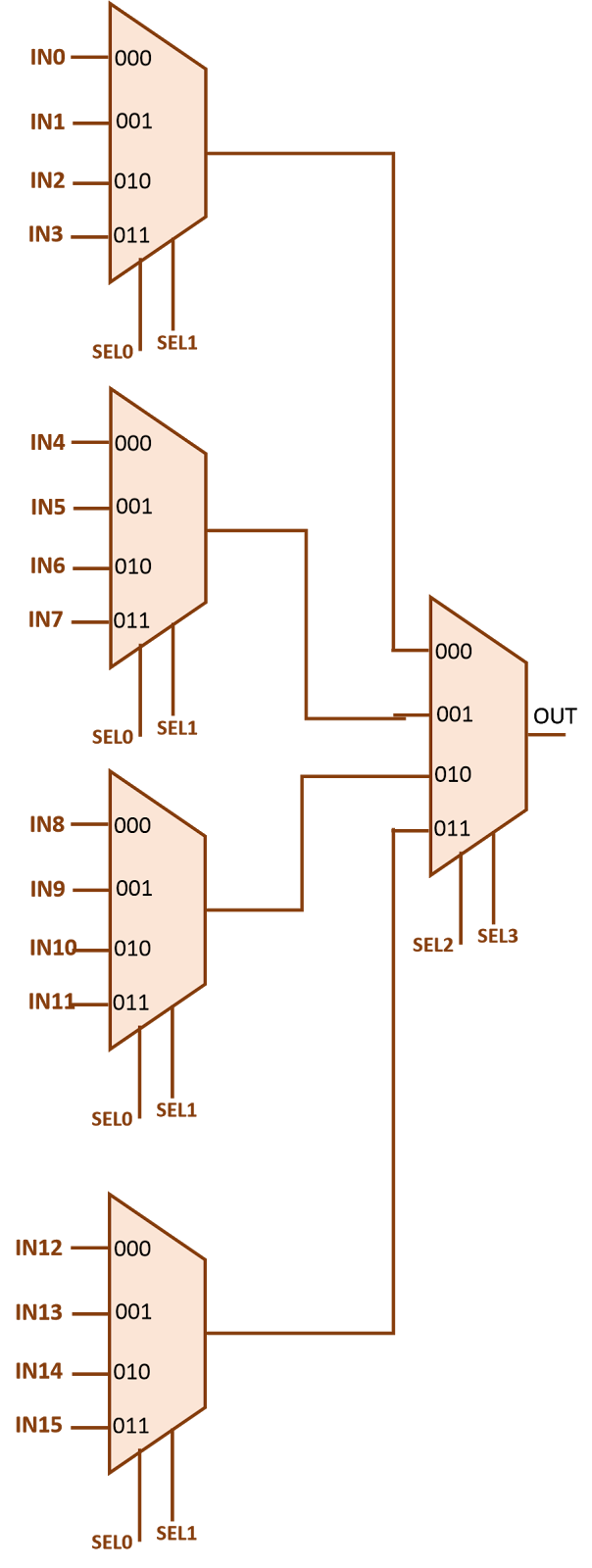
1. In the previous lab, we have learned how to simulate digital circuits using different types of modeling (i.e. Gate level, Data flow, Behavioral) in VeriLog. In this lab we will do more practice on combinational circuit simulation. Also, we will learn the hierarchical modeling (i.e. implement a larger module using a smaller module).

**1. Problem Description:**

Implement a gate level modelling of a 4x1 multiplexer. Further using the 4x1 MUX module, implement a 16x1 multiplexer.



**Sample Multiplexer Circuit**



**Sample 16X1 MUX**

**2. Problem Description:**

Consider the circuit diagram for full adder using a 3x8 decoder given below.

It takes 3-bit input number and produce Sum and Carry bit as an output

**Equation**

S(x, y, z) = ∑(1,2,4,7)

C(x, y, z) = ∑(3,5,6,7)





